CBCS SCHEME

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15EC61

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Hilbert transform. State the properties of it. **(04 Marks)**

b. Obtain the Hilbert transform of

i) $x(t) = (\cos 2\pi Ft + \sin 2\pi Ft)$

ii) $x(t) = c^{-j2\pi Ft}$ **(04 Marks)**

c. Explain canonical representation of band pass signal. **(08 Marks)**

OR

2 a. Derive the expression for the complex low pass representation of bandpass systems. **(08 Marks)**

b. For the given data stream 11011100. Sketch the line code

i) Unipolar NRZ

ii) Polar NRZ

iii) Unipolar RZ

iv) Bipolar NRZ **(04 Marks)**

c. Draw the power spectra of NRZ unipolar and NRZ polar format. **(04 Marks)**

Module-2

3 a. Show that the energy of a signal is equal to squared length of the signal vector. **(08 Marks)**

b. Obtain the decision rule for maximum likelihood decoding and explain the correlation receiver. **(08 Marks)**

OR

4 a. Explain the correlation receiver using product integrator and matched filter. **(08 Marks)**

b. Three signals $s_1(t)$, $s_2(t)$ and $s_3(t)$ are shown in Fig.Q.4(b). Apply Gram Schmidt procedure to obtain an orthonormal basis for the signals. Express signals $s_1(t)$, $s_2(t)$ and $s_3(t)$ in terms of orthonormal basis functions. **(08 Marks)**

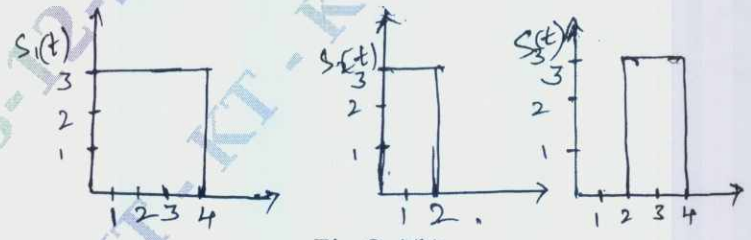

Fig.Q.4(b)

Module-3

5 a. With necessary diagrams, explain the generation and reception of BPSK signal. **(10 Marks)**

b. Given the binary data 10010011, draw the BPSK and DPSK waveforms. **(06 Marks)**

OR

6 a. Derive the expression for error probability of BFSK. (08 Marks)
b. With block diagram explain generation and detection of DPSK. (08 Marks)

Module-4

7 a. What is ISI? Obtain the expression of output of a filter with intersymbol interference. (08 Marks)
b. Explain the Nyquist criterion for distortionless baseband binary transmission and obtain the ideal solution for zero ISI. (08 Marks)

OR

8 a. Draw and explain the time-domain and frequency domain of duobinary and modified duobinary signal. (08 Marks)
b. What is channel equalization? With a neat diagram, explain the concept of equalization using a linear transversal filter. (08 Marks)

Module-5

9 a. Draw the 4 stage linear feedback shift register with 1st and 4th state is connected to Modulo-2 adder. Output of Modulo-2 is connected to 1st stage input. Find the output PN sequence and write the autocorrelation function with initial state 1000. (06 Marks)
b. Explain the generation of direct sequence spread spectrum with relevant waveforms and spectrums. (07 Marks)
c. Write a short note on application of spread spectrum in wireless LAN's. (03 Marks)

OR

10 a. With necessary block diagram, explain the transmitter and receiver of frequency hop spread spectrum. (08 Marks)
b. With a neat block diagram, explain the CDMA system based on IS-95. (08 Marks)

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15EC63

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the step-by-step CMOS P-Well fabrication process. **(08 Marks)**

b. With the mathematical equations, explain velocity saturation and mobility degradation effect due to increase in saturation current. **(08 Marks)**

OR

2 a. With the transfer characteristic of skewed inverter, explain the beta ratio effects. **(06 Marks)**

b. Compare CMOS and bipolar technologies. **(06 Marks)**

c. Consider the nMOS transistor in a 180 nm process with a nominal threshold of 0.4V and doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1V instead of '0'? **(04 Marks)**

Module-2

3 a. Discuss the λ-based design rules (i) Butting contact (ii) Transistors (nMOS, pMOS and CMOS) **(08 Marks)**

b. Derive the expression of delay interms of τ for CMOS inverter pair. **(08 Marks)**

OR

4 a. Draw the layout for $\overline{Y} = A + BC$ using CMOS. **(08 Marks)**

b. Find the C_{in} for the layout shown in Fig.Q4(b).

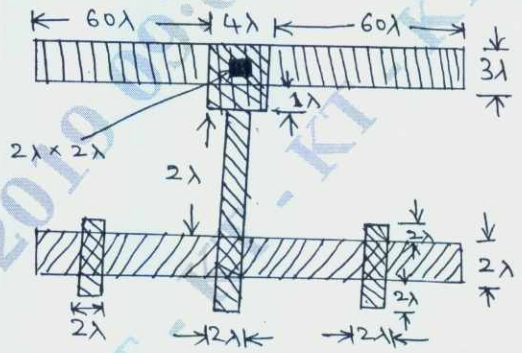

Fig.Q4(b) **(08 Marks)**

Module-3

5 a. Define scaling. Explain the scaling factors for device parameters. **(08 Marks)**

b. What is Manchester Carry Chain? Explain it. **(08 Marks)**

OR

6 a. What are the problems associated with VLSI design and how to reduce by using standard practice? **(06 Marks)**

b. Draw the 4 × 4 cross bar switch using MOS switches and explain it. **(06 Marks)**

c. Calculate the Regularity for 4 × 4 bit and 8 × 8 bit shifter. **(04 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: *Answer FIVE full questions, choosing one full question from each module.*

Module-1

1 a. Explain the following constraints imposed in real world circuits : (i) Noise margin (ii) Static levels (iii) Propagation delay (iv) Static and dynamic power consumption. **(08 Marks)**

b. Explain with illustration a simple methodology followed in IC industries. **(08 Marks)**

OR

2 a. Develop a verilog model for a 7 segment decoder. **(05 Marks)**

b. Develop a verilog model of a debouncer for a push button switch that uses a debouncer interval of 10 mS. Assume the system clock frequency is 50 MHz. **(05 Marks)**

c. Write a brief notes on finite state machine. **(06 Marks)**

Module-2

3 a. Design a 64 K * 8 bit composite memory using four 16 K×8 bit components. **(06 Marks)**

b. Explain the different ROM's used in digital system. **(06 Marks)**

c. Compute the 12 bit ECC word corresponding to the 8-bit data word 01100001. **(04 Marks)**

OR

4 a. Explain briefly about asynchronous static RAM. **(08 Marks)**

b. Develop a verilog model of a dual port, 4K ×16bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(05 Marks)**

c. Write a note on DRAM. **(03 Marks)**

Module-3

5 a. Explain briefly about the sequence of steps involved in IC manufacture. **(06 Marks)**

b. What are the distinguishes between a plat form FPGA from a simple FPGA? **(06 Marks)**

c. Explain the differential signaling. **(04 Marks)**

OR

6 a. Write a note on complex PLDs. **(08 Marks)**

b. Explain briefly about the internal organization of an FPGA with a neat diagram. **(08 Marks)**

Module-4

7 a. Explain the analog inputs used in input devices. **(04 Marks)**

b. Explain any four serial interface standards. **(08 Marks)**

c. Explain briefly the tristate buses and weak keepers. **(04 Marks)**

OR

8 a. Design and develop the verilog code for an input controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system. **(08 Marks)**

b. Show how 64-bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted. **(08 Marks)**

Module-5

9 a. Explain the hardware and software co design flow. **(08 Marks)**

b. Explain the design optimization that are must to meet the design constraints. **(08 Marks)**

OR

10 Write a short notes on :

a. Scan design and boundary scan. **(08 Marks)**

b. Built-In Self Test (BIST) **(08 Marks)**

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